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APPLICATION

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TITLE: SEMICONDUCTOR TRANSISTOR HAVING A POLYSILICON EMITTER AND METHODS OF MAKING THE SAME

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SEMICONDUCTOR TRANSISTOR HAVING A POLYSILICON EMITTER AND METHODS OF MAKING THE SAME

TECHNICAL FIELD

This invention relates to a semiconductor transistor having a polysilicon emitter and methods of making the same.

BACKGROUND

Transistors with polysilicon emitters generally have high current gains compared to transistors with metal emitters. FIG. 1 shows a conventional polysilicon emitter transistor 50. The polysilicon emitter 50 includes a collector region 52, a single crystal silicon base region 54, and an oxide layer 56. An emitter window 60 is created through the oxide layer 56 and is filled with an undoped polysilicon layer 58. Subsequently, the undoped polysilicon layer 58 is doped using ion implantation and annealed at a high temperature to diffuse the dopants onto the underlying single crystal silicon base region 54. Polysilicon emitter transistors may also be formed using an in-situ doped polysilicon layer.

However, as a result of the deposition of the polysilicon layer 58, the grain size of the polysilicon layer 58 may increase to the extent of forming a single crystal epitaxy. The grain size is illustrated in FIG. 1 where reference number 62 indicates a boundary between grains. Often, the grain size of the polysilicon layer 58 is comparable to the size of the emitter window 60. The grain size may limit the size of the emitter window 60 and thus may limit the size of the transistor device 50. In addition, the resulting grain size may have the undesirable effect of preventing uniform diffusion of dopants from the polysilicon layer 58 to the base region 54. The non-uniform diffusion of dopants may have a negative impact on the current gain of the

polysilicon emitter transistor 50. Moreover, the use of in-situ doped polysilicon may have an even greater negative effect on the current gain of the transistor 50 than the use of undoped polysilicon that is subsequently doped.

SUMMARY

The invention provides polysilicon-emitter transistor devices that overcome limitations of prior art devices. According to one aspect of the invention, a polysilicon emitter transistor includes a transistor having an emitter window exposing a base region of the transistor. A first polysilicon layer is deposited within the emitter window at least on the base region. An interfacial oxide layer is then formed, for example, by annealing the first polysilicon layer. Then, a second polysilicon layer is formed on the interfacial oxide layer.

In different embodiments, the emitter window may be approximately .1 to .2 μm wide, and the first polysilicon layer may be approximately 30 to 100 Angstroms (Å) thick prior to formation of the interfacial oxide. The interfacial oxide may be approximately 5 to 50 Å thick and can be thermally grown. The second polysilicon layer may be approximately 500 to 5000 Å thick and dopants can be ion-implanted in the second polysilicon layer. An annealing process may also be applied after deposition of the second polysilicon layer.

Advantages of the invention include one or more of the following. The polysilicon grain size in the region of the emitter adjacent to the base region is smaller, and because of this, smaller polysilicon-emiter transistors may be realized and the diffusion of dopants from the emitter to base is more uniform. The uniform diffusion of dopants also can increase the current gain and the speed of the transistor The interfacial oxide layer may also improve the flow of majority carriers through the emitter diffusion region and into the intrinsic base sub-region without having to heavily dope the intrinsic base sub-region. Also, transistors may be made with

a thinner emitter diffusion region and a narrower intrinsic base sub-region. As a result, the current gain and speed performance of the transistor may be improved without negatively impacting the resistance of the intrinsic base sub-region or the resistance of the emitter diffusion region.

The techniques disclosed are applicable to any polysilicon-emitter transistor device regardless of the type of dielectric or oxide layer deposited on the base region. The invention also applies to bipolar transistors used in bipolar-complementary metallic oxide semiconductors (Bi-CMOS) semiconductor devices.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a cross-sectional view of a prior art transistor.

FIGS. 2-4 are cross-sectional views depicting steps of manufacturing a transistor having a polysilicon emitter in accordance with the invention.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

FIG. 2 illustrates a cross-sectional view of an exemplary semiconductor device 100 at an intermediate step of forming a bipolar device having a polysilicon emitter in accordance with the invention. At this intermediate step, the semiconductor device 100 comprises a substrate 102 having a collector region 104, a base region 106 formed over the collector region 104, and an oxide region 108 formed over the base region.

In the exemplary embodiment, the collector region 104 is formed by masking the top surface of the substrate 102 to define the collector region, heavily doping the substrate 102 with n-doping material (e.g. phosphorous or arsenic) to form a diffused n-doped region, and then forming a lighter n-doped epitaxial layer above the heavily doped diffused region. The base region 106 may be formed of silicon, silicon-germanium, or silicon-germanium-carbon, and may be epitaxially grown and doped with p-doping material (e.g. boron).

In the exemplary embodiment, the oxide layer 108 can be a dielectric layer such as a single oxide layer, an oxide-nitride-oxide (ONO) stack, or other dielectric layer. For example, the oxide layer 108 can be implemented as an ONO stack comprising a lower silicon dioxide (SiO_2) layer 110 formed over the base region 106, a silicon nitride (Si_3N_4) layer 112 formed over the silicon dioxide (SiO_2) layer 110, and an upper silicon dioxide (SiO_2) layer 114 formed over the silicon nitride (Si_3N_4) layer 112.

The lower silicon dioxide (SiO_2) 110 may be grown or deposited, and is thereafter annealed. The thickness for the lower silicon dioxide (SiO_2) layer 110 may be approximately 30 to 200 Å. The silicon nitride (Si_3N_4) layer 112 may be deposited by low pressure chemical vapor deposition (LPCVD), atmospheric pressure chemical vapor deposition (APCVD), or plasma enhanced chemical vapor deposition (PECVD). The thickness of the silicon nitride (Si_3N_4) layer 112 may be approximately 50 to 1000 Å. The upper silicon dioxide (SiO_2) layer 114 is deposited by chemical vapor deposition (CVD) or plasma-enhanced chemical vapor deposition (PECVD), and may have a thickness of approximately 1000 to 5000 Å.

FIG. 3 illustrates a cross-sectional view of the exemplary semiconductor device 100 at a subsequent step of forming a bipolar device in accordance with the invention. In this subsequent step, standard photolithographic techniques are used to etch through the oxide layer 108 and create an emitter window 120. The emitter window 120 defines the intrinsic emitter, base and

collector regions of the device and may be approximately .1 to .2 μm wide as indicated by reference number 107.

FIG. 4 illustrates a cross-sectional view of the exemplary semiconductor device 100 at a subsequent step of forming a bipolar device in accordance with the invention. In this step, a first polysilicon layer is used to fill the emitter window 120 and at least on the base region. At this stage, this first polysilicon layer would consist of layers 123 and 124 of FIG. 4. However, as will be understood following later discussion, the first polysilicon layer is treated so that layer 123 remains as a polysilicon layer, but layer 124 is an interfacial oxide layer. The initially formed first polysilicon layer (which we will refer to as layers 123 and 124) may be un-doped and deposited using, for example, LPCVD, rapid thermal chemical vapor deposition (RTCVD), or other similar techniques. The first polysilicon layer 123 and 124 may have a thickness of approximately 30 to 100 Å. In another embodiment, the first polysilicon layer 123 and 124 may comprise an amorphous silicon layer.

Once the thickness of the first polysilicon layer 123 and 124 reaches a predetermined thickness value of approximately 30 to 100 Å, the deposition process is interrupted and oxygen is bled into a process chamber that is used during the deposition process. The details of bleeding oxygen into the process chamber are dependent on the design of the LPCVD or RTCVD reactor.

The bleeding of oxygen into the process chamber facilitates the oxidation of a portion of the first polysilicon layer 123 and 124 so as to form an interfacial oxide layer 124, and leaving the remaining layer 123 as polysilicon. The interfacial oxide layer 124 is thermally grown during a first anneal step to a thickness of approximately 5 to 50 Å. The temperature of the first anneal step should be higher than the temperature used during the deposition of the first polysilicon layer 123 and 124. The first anneal step facilitates the crystallization of the polysilicon so that a small grain size is formed in a lower region 128 that is adjacent to the

intrinsic base region 106a. If the initially deposited first polysilicon layer 123 and 124 is an amorphous silicon layer, then the first anneal step may convert the silicon into polysilicon and crystallize the lower region 128 of the silicon.

The first anneal process time can range from a few seconds to 150 minutes depending on the type of equipment used to perform the annealing. For example, in a furnace type reactor having a relatively large volume, the anneal temperature may be lower and the anneal time may be longer than another type of reactor. The temperature applied during the anneal process can range from 400° to 900° C and is also dependent on the type of reactor (e.g. epitaxial silicon deposition chamber, such as ASM Epsilon or Applied Materials Centura, or a RTCVD reactor).

Once the interfacial oxide layer 124 is formed, a second polysilicon layer 125 is deposited over the interfacial oxide layer 124. The thickness of the second polysilicon layer 125 is measured at a flat surface indicated by reference number 127 and is approximately 500 to 5000 Å. The second polysilicon layer 125 is deposited using the same techniques as are employed to deposit the first polysilicon layer 123. The second polysilicon layer 125 is either deposited in-situ doped or non-doped and then doped to achieve a certain conductivity. The doping material or dopants can include n-doping material such as phosphorus or arsenic if the device is a NPN type transistor. On the other hand, if the device is a PNP type transistor, then the doping material can include p-doping material such as boron.

A second annealing step can be applied to the second polysilicon layer 125 so as to drive the dopants from the second polysilicon layer 125, through the first polysilicon layer 123, and into the base region 106. In another embodiment, the second polysilicon layer 125 can comprise an amorphous silicon layer.

After doping the second polysilicon layer 125, the dopants diffuse thru the interfacial layer 124 and the first polysilicon layer 123 and into a portion of the base region 106, thus

forming an emitter diffusion region 126. The emitter diffusion region 126 thereby reduces the thickness of the base region 106 below the emitter diffusion region 126. The sub-region of the base region 106 below the emitter diffusion region 126 is termed herein as the intrinsic base sub-region 106a. The sub-region of the base region 106 not below the emitter diffusion region 126 is termed herein as the extrinsic base sub-region 106b.

The small grain size of the polysilicon at the lower region 128 facilitates the uniform diffusion of dopants into the intrinsic base region 106a. Reference number 62 refers to an upper region whose grain size is large in comparison to the lower region 128. The uniform diffusion of dopants can increase the current gain and the speed of the device 100.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, oxide layers other than oxide-nitride-oxide layers can be used in the invention. Accordingly, other embodiments are within the scope of the following claims.